

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

STEPHEN BOYD, ET AL.

Application No.: 09/752,541

Filed: December 29, 2000

For: **A Parser For Signomial And Geometric Programs**

Art Group: 2124

Examiner: Tuan A. Vu

**INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

06/27/2005 EAREGAY1 00000086 09752541

02 FC:1806

180.00 DP

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

The fee set in the amount of \$180.00 for submission of the Information Disclosure Statement is enclosed herewith. Please charge any additional fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Date:

6/23/05

Respectfully submitted,

  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Robert B. O'Rourke, Reg. No. 46,972

12400 Wilshire Boulevard, 7th Floor  
Los Angeles, CA 90025  
Telephone: (408) 720-8300

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

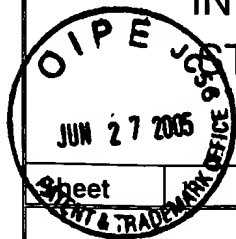
  
Carla Vignola

6-23-05  
Date

Substitute for Form 1449/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)


 Sheet  of  6
**Complete if Known**

Application Number	09/752,541
Filing Date	12-29-00
First Named Inventor:	Boyd, et al.
Art Unit	2124
Examiner Name	Tuan A. Vu
Attorney Docket Number	004363.P001

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)				
		US-	5,973,524	10/26/1999	Martin	
		US-	6,269,277 B1	07/31/2001	Hershenson	
		US-	4,827,428	05/02/1989	Dunlop, et al.	
		US-	6,381,563 B1	04/30/2002	O'Riordan, et al.	
		US-	6,532,569 B1	03/11/2003	Christen, et al.	
		US-	6,577,992 B1	06/10/2003	Tcherniaev, et al.	
		US-	6,425,111 B1	07/23/2002	del Mar Hershenson	
		US-	6,311,145 B1	10/30/2001	Hershenson	
		US-	6,581,188	06/17/2003	Hosomi, et al.	
		US-	6,311,315	10/30/2001	Tamaki	
		US-	6,002,860	12/14/1999	Voinigescu, et al.	
		US-	5,754,826	05/19/1998	Gamal, et al.	
		US-	5,633,807	05/27/1997	Fishburn, et al.	
		US-	5,055,716	10/8/1991	El Gamel	
		US-	5,289,021	02/22/1994	El Gamel	

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
		GB	2 131 228 A		6/13/1984	RCA Corporation		

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

*(use as many sheets as necessary)*

Application Number	09/752,541
Filing Date	12-29-00
First Named Inventor:	Boyd, et al.
Art Unit	2124
Examiner Name	Tuan A. Vu
Attorney Docket Number	004363. P001

of	6
----	---

[illegible]

Examiner  
Signature

Date Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

**If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.**

Substitute for Form 1449/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)		Application Number	09/752,541
		Filing Date	12-29-00
		First Named Inventor:	Boyd, et al.
		Art Unit	2124
		Examiner Name	Tuan A. Vu
		Attorney Docket Number	004363. P001
Sheet 1 of 6			

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		MEDIERO, F., et al., "A Vertically Integrated Tool For Automated Design Of Sigma Delta Modulators", IEEE Journal of Solid-State Circuits, Vol. 30., No. 7, July 1, 1995, pp. 762-767.	
		VON KAENEL, V., et al., "A 320MHz, 1.5mW at 1.36V CMOS PLL For Microprocessor Clock Generation", IEEE Solid-State Circuits Conference, November 9, 1996, Digest of Technical Papers, 42nd ISSCC96/ SESSION 8 / DIGITAL CLOCKS AND LATCHES / PAPER FA 8.2.	
		CHAN, et al., "Analysis of Linear Networks and Systems, " Addison-Wesley Publishing Company, 1972, pp. 23-25 and 46-57.	
		YOUNG, et al., "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessor", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1599-1607.	
		NOVOF, et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and $\pm 50$ ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30., No. 11, November 1995, pps. 1259-1266.	
		MOHAN, et al., "Simple Accurate Expressions for Planar Spiral Inductances", IEEE Journal of Solid-State Circuits, Vol. 34, No. 10, October 1999, pp. 1419-1424.	
		HERSHENSON, "CMOS Analog Circuit Design Via Geometric Programming", A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University, November 1999, 241 pages.	
		HERSHENSON, M., et al., "Optimization of Inductor Circuits via Geometric Programming", pp. 994-998, Design Automation Conference, June 21, 1999, Proceedings.	
		HERSHENSON, M., et al., "Automated Design of Folded-Cascode Op-Amps with Sensitivity Analysis", pp. 121-124, Electronics, Circuits and Systems, IEEE International Conference on LISBOA, September 7-10, 1998.	
		GIELEN, G., et al., "An Analogue Module Generator For Mixed Analogue/Digital ASIC Design", International Journal of Circuit Theory and Applications, Vol. 23, pp. 269-283, 1995.	
		KORTANEK, K.O., et al., "An Infeasible Interior-Point Algorithm For Solving Primal And Dual Geometric Programs," pp., 155-181, Mathematical Programming Society, Inc., 76:155-181, January 1, 1995.	

Examiner Signature	Date Considered
--------------------	-----------------

\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English Translation is attached.  
 This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.  
 If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Substitute for Form 1449/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE</b> <b>STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)		Application Number	09/752,541
		Filing Date	12-29-00
		First Named Inventor:	Boyd, et al.
		Art Unit	2124
		Examiner Name	Tuan A. Vu
Sheet <b>1</b>	of <b>6</b>	Attorney Docket Number	004363. P001
<b>NON PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.	
		HERSHENSON, M., et al., "Posynomial models for MOSFETs" 9 pages, July 7, 1998.	
		CHANG, H, et al., "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits" 6 pages, IEEE 1992 Custom Integrated Circuits Conference.	
		CHAVEZ, J., et al, "Analog Design Optimization: A Case Study" 3 pages, IEEE, January 1993.	
		GEILEN, G., et al., "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", pp. 707-713, IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, June 1990.	
		FISHBURN, J, et al., "TILOS: A Posynomial Programming Approach to Transistor Sizing" pp. 326-328, IEEE, 1985.	
		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
		SWINGS, K., et al., "An Intelligent Analog IC Design System Based On Manipulation Of Design Equations" pp. 8.6.1- 8.6.4, IEEE 1990, Custom Integrated Circuits Conference.	
		NESTEROV, Y., et al., "Interior-Point Polynomial algorithms in Convex Programming" 8 pgs., 1994, Society for Industrial and Applied mathematics.	
		YANG, H.Z., et al., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis" pp. 571-575, IEEE, 1996.	
		WONG, D.F., et al., "Simulated Annealing For VLSI Design" 6 pages, 1998, Kulwer Academic Publishers.	

Examiner Signature	Date Considered
--------------------	-----------------

\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Substitute for Form 1449/PTO  <h2 style="text-align: center;">INFORMATION DISCLOSURE</h2> <h3 style="text-align: center;">STATEMENT BY APPLICANT</h3> <p style="text-align: center;"><i>(Use as many sheets as necessary)</i></p> <div style="display: flex; align-items: center;"> <div>           Sheet <u>5</u> of <u>6</u> </div> </div>		<div style="text-align: center; border-bottom: 1px solid black; margin-bottom: 5px;"><b>Complete if Known</b></div> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Application Number</td> <td>09/752,541</td> </tr> <tr> <td>Filing Date</td> <td>12-29-00</td> </tr> <tr> <td>First Named Inventor:</td> <td>Boyd, et al.</td> </tr> <tr> <td>Art Unit</td> <td>2124</td> </tr> <tr> <td>Examiner Name</td> <td>Tuan A. Vu</td> </tr> <tr> <td>Attorney Docket Number</td> <td>004363. P001</td> </tr> </table>		Application Number	09/752,541	Filing Date	12-29-00	First Named Inventor:	Boyd, et al.	Art Unit	2124	Examiner Name	Tuan A. Vu	Attorney Docket Number	004363. P001
Application Number	09/752,541														
Filing Date	12-29-00														
First Named Inventor:	Boyd, et al.														
Art Unit	2124														
Examiner Name	Tuan A. Vu														
Attorney Docket Number	004363. P001														
<b>NON PATENT LITERATURE DOCUMENTS</b>															
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>												
		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.													
		OCHOTTA, E, et al., "Synthesis of High -Performance Analog Circuits in ASTRX/OBLS" pp. 273-295, IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 15, No. 3, March 1996.													
		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, <a href="http://www.siam.org/books/wright">http://www.siam.org/books/wright</a> , Printed August 19, 1998.													
		SHYU, J., et al., "Optimization-Based Transistor Sizing" pp. 400-408, IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1998.													
		WRIGHT, S., "Primal-Dual Interior-Point Methods" 14 pages, 1997, Society for Industrial and Applied Mathematics.													
		VAN LAARHOVEN, P.J.M., et al., "Simulated Annealing: Theory and Applications" 26 pages, 1987, Kulwer Academic Publishers.													
		HERSHENSON, M., et al., "CMOS Operational Amplifier Design and Optimization via Geometric Programming" pp. 1-4, Analog Integrated Circuits, Stanford University.													
		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.													
		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Design.													
		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.													
		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.													

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English Translation is attached.  
 This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.  
 If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Substitute for Form 1449/PTO		<b>Complete if Known</b>		
<b>INFORMATION DISCLOSURE</b> <b>STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)		Application Number	09/752,541	
		Filing Date	12-29-00	
		First Named Inventor:	Boyd, et al.	
		Art Unit	2124	
		Examiner Name	Tuan A. Vu	
Sheet	of	6	Attorney Docket Number	004363.P001
<b>NON PATENT LITERATURE DOCUMENTS</b>				
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>	
		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.		
		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.		
		BOWMAN, R., "An Imaging Model For Analog Macrocell Layout Generation", IEEE International Symposium On Circuits And Systems, Vol. 2, 8 May 1989, pp. 1127-1130, XP010085007.		
		HUNTER, A., et al., "Combining Advanced Process Technology and Design for Systems Level Integration", IEEE Proceedings, pages 245-250, First International Symposium On Quality Electronic Design, March 20, 2000		